Improved Design of 1T Charge-Modulation Pixel Structure for Small-Size and Low-Dark-Current Achievements

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Abstract

A ring-gate design of 1T (single-transistor) charge-modulation pixel structure is proposed. It obviates the need to employ STI (shallow trench isolation) for avoiding crosstalk. This enables achievements of smaller pixel size and/or higher fill factor. It also reduces dark current by limiting peripheral leakage current contribution and minimizing band-to-band tunneling effect. A test chip integrating an array of 1.4µm-pitch, 50%-fill-factor pixels is designed in a 0.13µm CMOS technology. The measured pixel characteristics are compared with those from a 2.2µm-pitch, 46%-fill-factor previous design (also in a 0.13µm CMOS process). The comparison shows that the 1.4µm-pitch ring-gate pixel has an improved conversion gain (CG) and a degraded full well capacity (FWC). It also shows substantial reductions on dark current, temporal noise and FPN. The resulting signal-to-noise ratio outweighs degradation of FWC, which also improves dynamic range.

1. Introduction

There have been rapid developments on CMOS image sensors to meet requirements of the fast growing market. Important R&D efforts have been focused on pixel-pitch reduction for higher image resolution and/or higher density of integration. In this miniaturization race [1]-[3], one effective approach consists in employing fewer transistors for active pixel sensors (APS) by sharing pixel components. This has led to suggestions of 2.5T, 1.75T and 1.5T architectural configurations as well as recent 1.4µm-pitch achievements [4].

Also in the attempt of minimizing the number of pixel components, the 1T charge-modulation pixel structure has been proposed and investigated [5]-[8]. It appears promising for pixel size reduction, because the pixel contains only a single transistor to combine the pixel operations: photodetection, charge integration, signal readout and reset.

2. 1T Charge-Modulation Pixel Structure

The 1T charge-modulation pixel contains only one NMOS transistor. The transistor structure differs from the conventional one mainly in that it is on a floating P-well with controlled doping profile. A potential well beneath the transistor channel can be formed to store a charge packet (holes) coming from photo-generation of electron-hole pairs. The I-V characteristics of the transistor are thus modulated by the stored charge, which is related to the light intensity received on the sensing surface of the pixel. The basic structure of the 1T charge-modulation pixel is shown in Fig. 1.

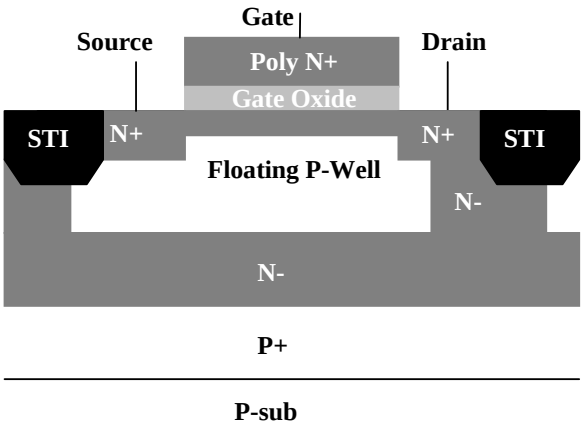

Fig. 1. Cross-section view of the 1T charge-modulation pixel structure

This 1T charge-modulation pixel operates with 3 phases: integration, readout and reset, which can be described as follows.

In the integration phase, a low voltage level is applied to the gate of the transistor to turn it OFF. In such a bias condition the body of the transistor exhibits a potential well in the well region for storing holes (see Fig. 2a). When the pixel is under illumination, light penetrates through the gate and is absorbed in the transistor body. Photo-generated electron-hole pairs are separated due to built-in electrical field in the body. The electrons are swept away mainly to the drain, while the holes are collected and accumulated in the potential well. The stored positive charge increases the potential of the transistor body, leading to a decrease of the transistor threshold voltage V_{th} [7].

In the readout phase, the transistor is switched ON by applying a gate voltage higher than the maximum V_{th} in dark conditions. It operates as a source follower with fixed gate and drain voltages. The decrease of V_{th} reflecting the amount of the stored charge is sensed as an increase of the source voltage. The source voltage is then readout by double sampling to suppress V_{th} dispersion and thus to reduce fixed pattern noise (FPN).

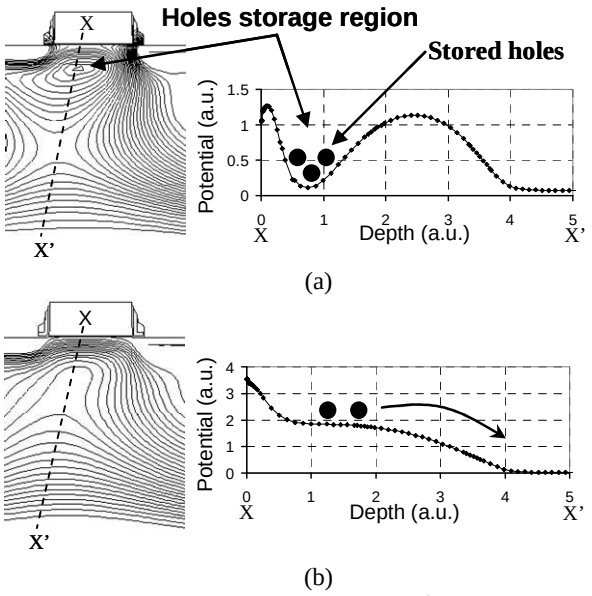

Fig. 2. Simulation with ISE TCAD. a) Potential profile in integration phase forming a well for storing holes; b) Potential profile for reset period with evacuation of stored holes

For the reset of the pixel, a still higher voltage is applied to the transistor gate. At the same time, the source voltage is clamped to the drain voltage to minimize channel current. Under this high gate voltage, the potential profile of the transistor body becomes monotonic decreasing (see Fig. 2b). The potential well disappears and the stored holes are pushed away to the substrate. Fig. 3 shows the timing waveforms of the pixel and sampling signals.

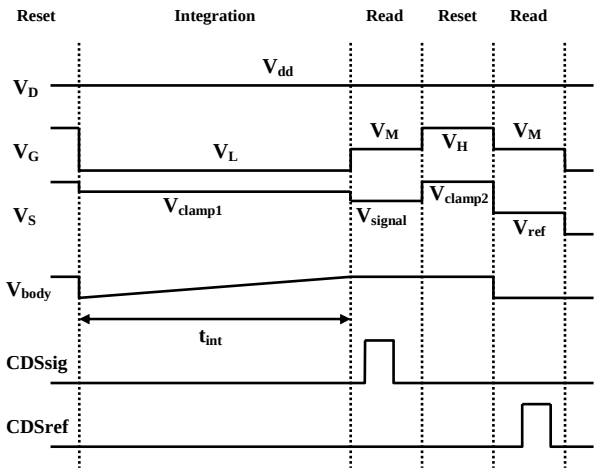

Fig. 3. Timing diagrams

This 1T pixel structure has a conversion gain defined as the pixel output voltage read for each photo-generated and stored hole (in $\mu V/h^+$). It is a key parameter related to performances such as responsitivity and signal-to-noise ratio. By modeling the device operation, it can be expressed as:

$$CG = \frac{qA_v C_{dep}}{C_{ox} C_{B'}} \qquad (1)$$

where A_v is the gain of the source-follower slightly lower than unity, C_{dep} is the depletion capacitance under gate between the floating transistor body node B' and the Si/SiO_2 interface, C_{ox} the gate oxide capacitance, and $C_{B'}$ the total body capacitance between node B' and ground. Roughly, with simplifying assumption for $A_v \approx 1$ and $C_{ox} \approx C_{B'}$, the conversion gain can be estimated by:

$$CG \approx q / C_{ox} . \qquad (2)$$

Another important parameter of the pixel is its charge-handling capability, also defined as full well capacity (FWC). It corresponds to the maximum amount of charge Q_{sat} that can be stored in the potential well without spread, minus reset residual charge Q_{rst} (that may cause image lag).

Both above parameters are involved in the setting of the dynamic range. Since they are surface-dependent, it can be expected that reducing pixel size will enhance CG on the one hand, and degrade FWC on the other.

3. Physical Design

We have recently designed the 1T charge-modulation pixel structure in a 0.13µm CMOS process [8]. The layout of the transistor was a conventional form with a gate area of 1µm x 1µm. To avoid crosstalk, both source and drain areas of the transistor were surrounded with STI (shallow trench isolation), as is shown in Fig. 1. The pixel size was a 2.2µmx2.2µm, with a 46% fill factor.

By analyzing this 2.2µm-pitch pixel design, we have noticed that the use of STI in the pixel also presents drawbacks. Firstly, it increases the pixel size and reduces the fill factor. Secondly, it increases peripheral leakage current at the silicon surface and its contribution to the pixel dark current.

On the other hand, a conventional rectangular-gate transistor is not suitable to minimize tunneling effects (band-to-band tunneling or/and trap-assisted tunneling, impact ionization) in high-doping pn junction areas. By characterizing the 2.2µm-pitch pixel, we have observed a sharp increase of dark current for the drain voltage of the transistor beyond a certain threshold value, which is due to the band-to-band tunneling effect (shown in Fig. 4). It occurs in the gate-to-drain overlapped surface area where high-doping-profile and high-electric-field conditions are met. Such conditions are first met near sharp corners of the drain area. Predictably, this tunneling effect may be more pronounced when reducing the pixel size.

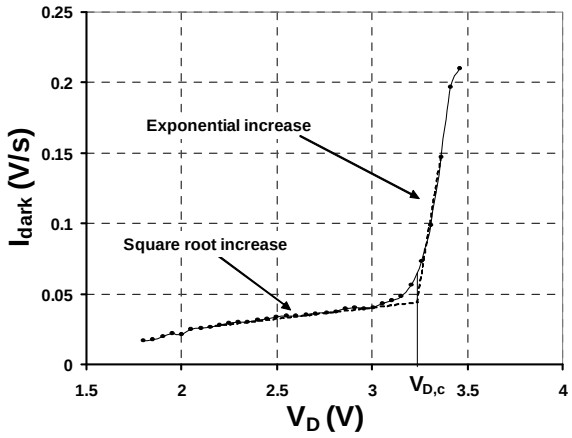

Fig. 4. Measured dark current of a 2.2µmx2.2µm rectangular-gate pixel versus drain voltage VD

To minimize this effect, we suggest a ring-gate design with source at the center and peripheral drain (see Fig. 5).

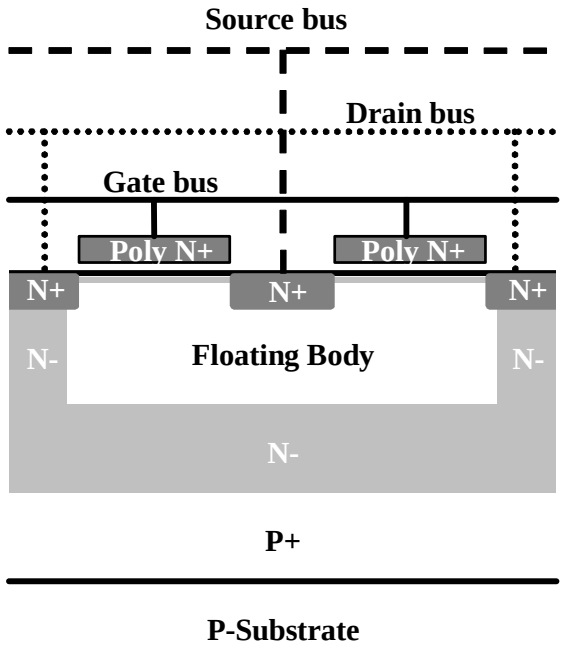

Fig. 5. Cross-section view of the ring-gate 1T Charge-modulation pixel

This implementation also eliminates the need for STI and its resulting dark-current contribution, because the surrounding drain of the transistor in the peripheral pixel area prevents charge diffusion. This STI suppression allows pixel-size reduction and/or fill-factor improvement.

Fig. 6 shows a 1.4µm-pitch, ring-gate pixel array designed in a 0.13µm front-end based CMOS process & 90nm copper-based process. The pixel has a 50% fill factor.

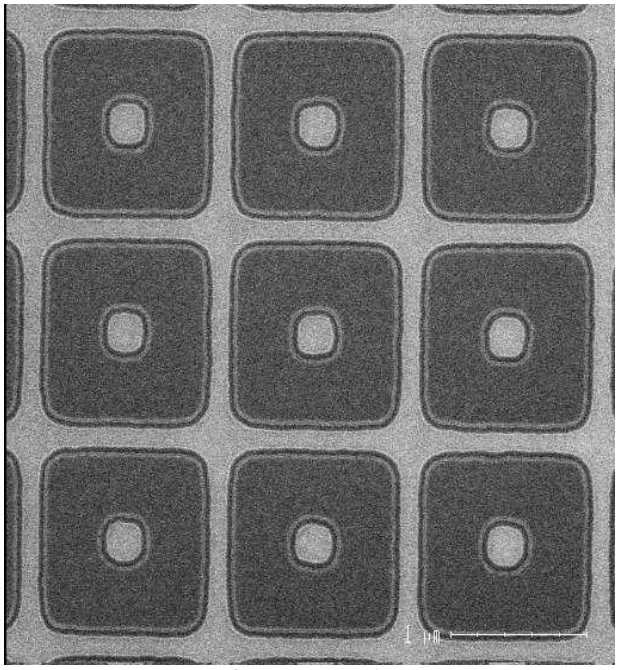

Fig. 6. Microphotography of a pixel array before metallization process (by Scanning Electronic microscope)

4. Pixel Characteristics

Fig. 7. shows a test chip integrating an array of 1.4µm-pitch pixel. It has been fabricated using a 0.13µm Front-End CMOS process that has the following characteristics: P-substrate, STI isolation (for peripheral region only), twin well, double gate oxide, and single poly. Unsilicided contacts have been used in the pixel arrays for higher integration density. The pixel fabrication process requires only 3 extra masks for specific implants and is fully compatible with the CMOS digital process.

Fig. 7. Microphotograph of a fabricated Test Chip

The measured characteristics of the 1.4µm-pitch ring-gate pixel are compared with those of the previously-designed 2.2µm-pitch pixel (summarized in Table 1).

The comparison of results in Table 1 shows improvements in most aspects (apart from FWC and sensitivity) for the 1.4µm-pitch ring-gate design. As expected, CG is enhanced while FWC is degraded. Meanwhile, the dark current is lowered from 80aA/pixel ($500h^+/s$) to 6.4aA/pixel ($39.7h^+/s$), which means a more than 12-fold reduction. Noise aspect including temporal noise and FPN is also substantially improved. One can also notice that a larger dynamic range is reached, meaning that the improvement on signal-to-noise ratio outweighs the degradation of FWC. However, many other improvements have still to be made (by design and process optimization) on this kind of architecture so as to reach performances (such as full well capacity, sensitivity, …) of current pixels employed in the image sensor application fields.

An example of image taken with this test chip is shown in Fig. 8.

Table 1. Comparison of measured characteristics between the 2.2µm rectangular-gate pixel and the 1.4µm ring-gate-design pixel

Parameter	2.2µm-pitch rectangular-gate	1.4µm-pitch ring-gate	Testing conditions
Process	0.13µm 1P 4M CMOS	0.13µm FE + 90nm BE 1P 3M CMOS	
Test chip size	3.2mm x 3.2mm	3.0mm x 3.2mm	
Pixel size	2.2µm x 2.2µm	1.4µm x 1.4µm	
Resolution	CIF (352 x 288)	VGA (672 x 512)	
Fill factor	46 %	50 %	Without microlens
Supply voltage	1.2V / 3.3V	1.2V / 3.3V	
Conversion gain	35µV/h^+	**58**µV/h^+	
Full well capacity	6200 h^+	**2000** h^+	
Dark current	500 h^+/s	**39.7** h^+/s	Mean value @ RT
Pixel temporal Noise	6 h^+	**2.4** h^+	In darkness
FPN	21.3 h^+	**4.3** h^+	Without additional correction circuit
Noise floor	40 h^+	**4.9** h^+	Temporal noise, FPN & DSNU in darkness
Dynamic range	44 dB	**52** dB	Usable Well over Noise floor
Sensitivity	1800 h^+/lux.s	600 h^+/lux.s	B/W sensitivity without microlens Halogen 3200K IR cut off 650nm

Fig. 8. Image example using the test chip (VGA format)

5. Conclusion

We have proposed a ring-gate design of the 1T charge-modulation pixel structure. It suppresses the need to employ STI in the pixel, thus allowing smaller size and/or higher fill factor. This also reduces dark current by limiting peripheral leakage current and minimizing band-to-band tunneling effect.

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